

Seeking workable low-cost silicon carbide

Material properties suggest high temperature and power electronics could be well served by silicon carbide (SiC), but many production difficulties have blocked the easy paths to adoption. However, SiC deposited on a silicon substrate has many attractions from a volume production perspective. **Dr Mike Cooke** reports on Japanese and US efforts to make this a viable option.

Silicon carbide has many promising properties from an electronics perspective: high thermal conductivity, high breakdown field, and high mobility given the high breakdown field (see Table). High thermal conductivity is particularly attractive for components operating at higher temperatures or needing to dissipate power.

The various branches of the US military have been some of the long-term supporters of SiC research. Much of the equipment used in warfare, such as rockets and jet engines, run extremely hot. It is estimated that more than 50% of the air-conditioning effort on fighter planes is designed to cool the avionics, not the pilot. Other military fields where high-temperature ICs could be of interest are armored vehicles and missile control.

There is also commercial interest for applications in hot environments such as diesel-electric locomotives and automobiles. Engine-control computers in automobiles are presently located in passenger areas rather than under the hood due mainly to the temperature constraints of silicon technology. The high breakdown voltage suggests application to inverter devices, as used in air-conditioners and refrigerators, along with power devices in personal computers and home electric appliances.

However, despite the US Army spending some \$2bn on SiC research, the results have not been particularly good, and a diminishing returns effect has been seen.

The research focus is still on the simpler power components, where the material offers theoretical advantages.

SiC's application sees problems arising in one of its most basic semiconductor structures — the pn junction. These problems arise, as with so many other semiconductor materials (e.g. gallium nitride), in various forms of defect. It is found that the performance of a device based on a SiC pn junction degrades when the bias moves from one direction to the other, and that the effect is cumulative. Schottky diodes (metal-semiconductor junctions) are less affected. One main difference between these structures is that pn junction operation depends on minority carriers, while Schottky junction currents are dominated by majority carriers. SiC has therefore seen some success in the Schottky diode arena, particularly for those used in power factor correction devices to improve cost efficiencies in office automation products. When MOSFETs are constructed in SiC, it's common to include Schottky diodes to protect the pn junctions from performance-degrading bias reversals.

Production nightmares

The main problem with producing SiC devices is the extreme difficulty in producing suitable, low-defect substrates. Silicon carbide does not have one simple crystal structure — rather, there is a whole zoo of 'polytypes' of hexagonal (6H, 4H, 2H), cubic (3C) and rhombohedral (15R) forms that can arise. In addition,

Table. Comparison of material properties. SiC properties depend on polytype: ranges include 3C, 4H, 6H. Polytype 3C is at lower end of energy gap (E_g), breakdown field (E_b) and thermal conductivity (λ), while its electron mobility (μ_e) is around $800\text{cm}^2/\text{V-s}$. Linear thermal expansion coefficient (LTEC) comes from [1], while other values are from [2].

Material	E_g (eV)	E_b (MV/cm)	λ (W/cm-K)	μ_e ($\text{cm}^2/\text{V-s}$)	LTEC ($\times 10^6\text{K}^{-1}$)
SiC	2.4–3.2	1–5	3.6–4.9	400–900	4.5
Si	1.12	0.25	1.3	1350	3.6
GaN	3.4	~5	2.0	1000–1350	5.6 (3.2)
AlN	6.2	1–2	2.85	300	5.3

silicon carbide does not have a liquid state except at very high pressure (>30 bar). The sublimation temperature (gas–solid transition) of SiC is well above the melting point of silicon (1420°C). This all makes control of the crystal growth process near to impossible. Most defects are related to the very high temperatures (1600–2500°C) needed to produce SiC crystals. The higher the temperature, the more defects are formed. Further, SiC is second only to diamond in hardness, making machining (polishing, grinding) of wafers very difficult.

One major SiC defect has been micropipes, which can be seen as being analogous to the streams of bubbles that emanate from nucleation centers in a pan of boiling water. When, in addition, one attempts chemical vapor deposition (CVD) epitaxy on top of a surface with micropipes, the open spots affect the deposition and one ends up with a 'Swiss cheese'-like layer of SiC. Most attempts to deal with micropipes have centered on slowing down bubble nucleation on the growing SiC surface. However, Cree, the supplier of the majority of SiC substrates, recently announced the commercial release of 'Zero Micropipe (ZMP)' 100mm wafers.

Looking for lower costs, higher volume

Production difficulties naturally translate into high cost and low technology uptake. Looking for lower-cost SiC, some researchers are developing silicon carbide layers on low-cost silicon. A further advantage of silicon is the possibility of making devices in far higher volume, since silicon wafers extend up to 300mm in diameter rather than the 100mm maximum of Cree's products. For sure, one loses SiC's thermal conductivity advantage, but thinning of wafers before packaging is a standard technique used in silicon processing to both reduce the size of components and increase thermal conduction.

Two firms following the SiC/Si approach with a view to low cost and high volume are Covalent in Japan and C9 in the USA. Covalent, formerly Toshiba Ceramics, has this year become independent of its parent company in one of the many recent reorganization efforts in the Japanese business landscape. C9 is a company that largely works on US defense R&D contracts.

SiC has been put on silicon before, usually in the cubic '3C' polytype. This is often performed by a carbonization process to create a buffer layer to bridge the 20% lattice mismatch between Si and SiC that normally leads to a high level of defects and consequent reduction in electronic performance [3]. One of the main problems of carbonization is the formation of voids in the substrate when the carbon supply is insufficient to form an adequate buffer layer. Another problem is that the buffer layer forms in islands that are not correctly oriented with respect to each other — in 'twinning' and 'antiphase' configurations — for

forming a high-quality SiC film. Optimization of the C:Si ratio is needed to produce the best-quality 3C SiC. High temperatures increase the growth rate, but the resulting material is usually not good enough for producing electrical devices due to high defect rates, although micromechanical systems have been produced using the etch selectivity between the two materials.

MOVPE 3C SiC/Si

In 2004, Toshiba Ceramics announced development of wafers with a cubic silicon carbide single-crystal film grown on a silicon substrate, using metal-organic vapor phase epitaxy (MOVPE). The firm reported that it had put a compound semiconductor buffer layer film with the same crystal form as silicon and silicon carbide between the silicon carbide and the silicon substrate to significantly reduce the crystal defects caused by the 20% SiC/Si mismatch. The aim was production on 6-inch or more diameter wafers of a cubic silicon carbide film for a comparatively low price with reliable quality. Another aim would be to insert such wafers into standard silicon device manufacturing lines. Toshiba Ceramics also hoped that the high-quality SiC layers on SiC could be used in the development of nitride semiconductor devices.

Hideo Nakanishi of Covalent's Core Technology Center comments: "We made every effort to develop SiC-on-Si substrates for power devices. However, nitride semiconductor materials are now in strong demand from many device makers. Therefore, we started GaN-on-Si substrate development. We have recently demonstrated that SiC is a useful buffer material for GaN crystal growth on Si substrates. Now, we are developing GaN/SiC/Si substrates for power high-electron-mobility transistor (HEMT) devices alongside SiC-on-Si substrate development."

Based on research reported last year [1, 4], Covalent researchers believe that GaN grown on 3C SiC on silicon wafers is a 'promising' route to power HEMT

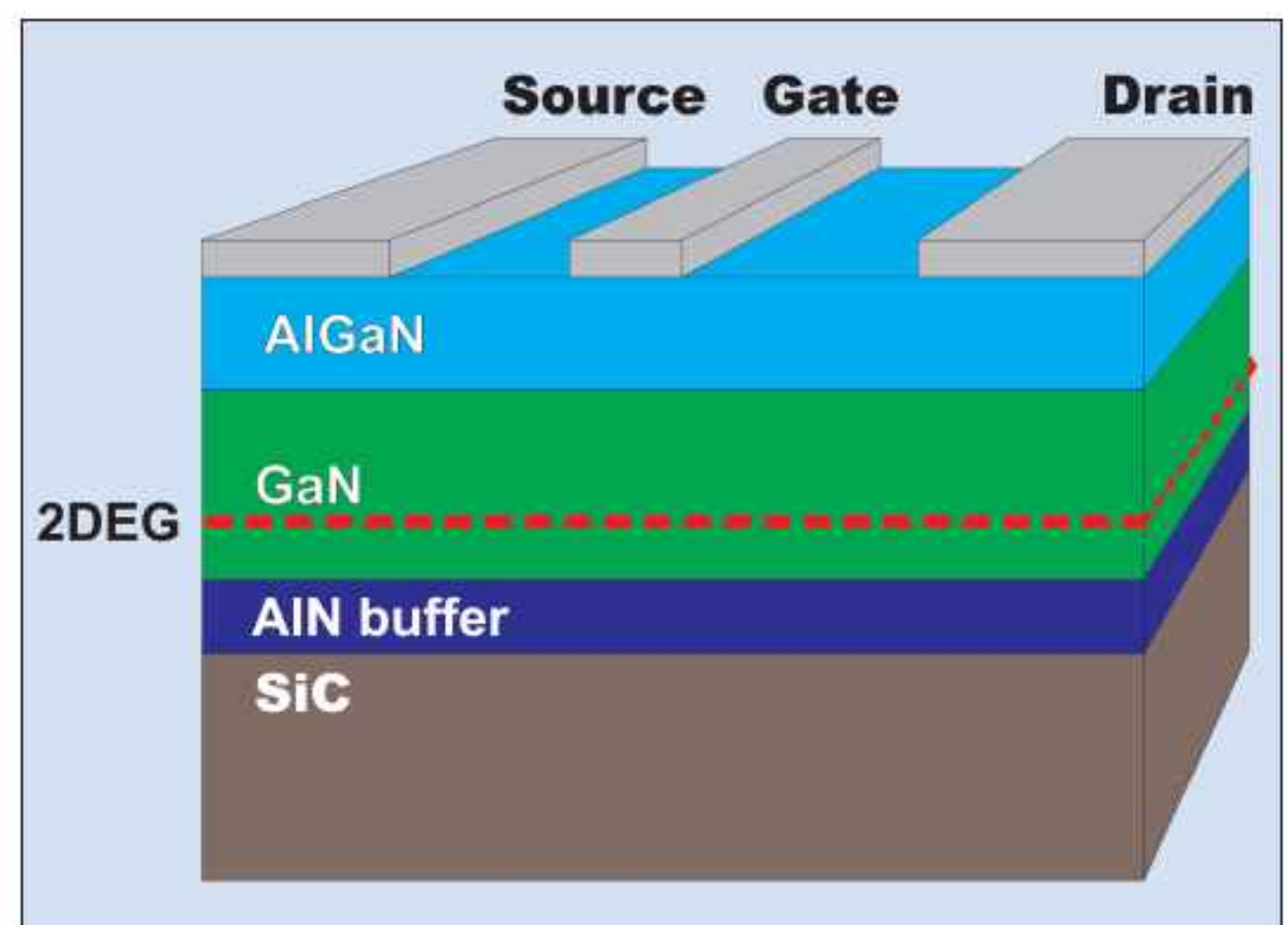


Figure 1. Schematic of GaN/SiC HEMT.



Figure 2. Covalent's GaN/SiC/Si layer structure with AlN buffer. The SiC crystal structure is oriented [111] and the xN [0001].

devices operating at high frequency at lower cost.

In particular, Covalent has seen GaN layers up to 3 μm thick with reduced levels of cracking and has measured the respective polarities of the interfaces, finding that the GaN–SiC interface has the correct Ga and Si polarities for creating the two-dimensional electron gas (2DEG) needed for HEMT device operation (Figure 1).

The cracking of hexagonal GaN (wurzite) on Si is a particular problem due to the large mismatches in both the lattice constant (17%) and the thermal expansion coefficient (33%). In contrast, the 3C SiC/GaN mismatch is 3%. The polarity characteristics of the GaN–SiC interface were determined using convergent beam electron diffraction (CBED). The MOVPE growth was on 3-inch (111) silicon substrates in a horizontal reactor. A thin AlN layer is interposed between the GaN and SiC to prevent unwanted Ga–Si interactions (Figure 2).

More recently, electrical characterizations have been performed on GaN and SiC Schottky contacts. The GaN contact was found to have a breakdown voltage of 250V, while on SiC it is 200V. The leakage currents are described as being 'low' in the case of GaN and 'high' for the SiC contact. The SiC leakage is provisionally blamed on 'antiphase' domains and stacking faults.

Superlattice SiC

C9 claims that its proprietary process is essentially micropipe free, being of the order of that in silicon (i.e. practically non-existent). The technology developed from work on silicon-on-insulator epitaxy over a period of about 10 years. Part of the advantage of C9's process comes from its use of atomic layer deposition on silicon substrates. This can form superlattices of SiC with varying levels of carbon (from 0% up to 40–50%). However, problems arise with going beyond a carbon content of 50%; C9's chief technology officer, CG Wang, has found during many years of research into growing diamond crystal that the process tends to deposit as graphite rather than diamond. C9 grows layers up to 100nm thick. One can also include doping elements as the growth progresses. Doping can vary majority carrier densities from intrinsic semiconductor up to a carrier density of $10^{22}/\text{cm}^3$ (p or n). Since the

doping is carried out at the atomic level, one can achieve very sharp junction profiles compared with diffusion. Since one is building superlattice structures, the energy band gap is tunable.

According to the company, the electron mobility is of the order of $1000\text{cm}^2/\text{Vs}$ and the breakdown voltage is the same or better than for traditional SiC. The company attributes this to reduced defect levels.

Since C9 is starting from a silicon substrate using standard processes and tools, the starting costs are much lower than for those using expensive SiC substrates. However, being based on atomic layer deposition, the process is very slow. To achieve productivity increases, one needs to expand laterally to larger wafers. C9 has had a 6" (150mm) machine working since June 2006 and is starting work on scaling up to 8" (200mm). Chief executive officer Kevin Donegan believes that C9 could have an 8" machine working by June 2008 and that C9's techniques are scalable to the largest-diameter silicon wafers of 300mm and beyond (e.g. the 18"/450mm presently being touted in the industry as the 'next step up'). Along with this, C9 will work to improve quality, reducing defects even further.

Being based on ALD, C9's epitaxial structures are 'nano-engineered'. Donegan comments: "C9's material

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is a truly engineered material. The SiC resulting from other processes is God-made, because the temperature and other factors are almost impossible to control — one just has to pray that it doesn't go wrong."

C9 sees many possible applications for its materials, but has decided to focus on just a few. First are large-area Schottky diodes, since this is a well-established

SiC application. C9 plans to move from its present 1cm^2 Schottky diode products to 4cm^2 and eventually to whole wafer-area devices. Its Schottky diode structures can support current densities in the range $100\text{--}200\text{A}/\text{cm}^2$, so a 4cm^2 device could handle 800A. While great claims have been made for SiC elsewhere, the present reality is that single devices are generally rated at currents of 35–40A. Donegan believes that higher rated diodes ($\sim 75\text{A}$) are in fact multi-die products. Following on from Schottky diodes, pn junction diodes are planned, since C9's methodology should avoid the degradation seen in devices produced on standard SiC.

Another target is solar cells, particularly for hot environments (e.g. in Iraq) where amorphous silicon-based photovoltaics do not perform well. Logically, SiC solar cells could operate up to 600°C . C9 is looking to

produce multi-junction photovoltaic devices, with each junction centered on a different part of the available solar spectrum. Here, a tunable band gap comes in very handy. The standard SiC band energy comes in the large-energy photon ultraviolet range. Narrower gaps can scoop up the lower-energy photons into different 'buckets'.

At Boeing Spectrolab, compound semiconductor multi-junction solar cells have reached 40% efficiency. C9 believes that its single-crystal superlattice is at an advantage over multi-junction devices constructed out of conflicting materials. C9's structure consists of numbers of superlattice SiC layers with different band gaps connected in series with conducting tunnel diode junctions. The firm will be working with The Solar Energy Consortium (TSEC) in New York state, which has recently been allotted \$4m in US federal funds from the 2008 Defense Appropriations bill. It is hoped that the consortium will start by creating between 300 and 500 jobs after C9 has researched the technology.

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Beyond this, C9 is researching producing radio frequency devices based on high-electron-mobility transistors (HEMT). Another area is switching circuits. The most common structure for SiC switch devices is the junction gate field-effect transistor (JFET) in combination with silicon MOSFETs. The SiC power JFET combines a simple robust structure with high breakdown voltage and high speed. The SiC JFET Si MOSFET combination allows operation up to 175°C. If the SiC JFET could be released from the silicon temperature range, one could have devices operating in the 150–350°C range using standard packaging. One of the difficulties of producing high-performance SiC devices is making contact pads. With C9's ALD process, this can be overcome by first depositing a silicon layer and then the contact pad.

Donegan comments that limiting applications to power devices limits the possibilities to less than 10% of the total semiconductor market. C9 believes it can produce robust, rad-hard integrated circuits in SiC that could operate at much higher temperatures. ■

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